

LAST - [resistor.wsp:1] File View Edit Tools Window Help

Drafts
Pending
Active

L1: (105747) nonvolatile or (non adj volatile)
L2: (4626) 1 and (floating adj gate).clm.
L3: (829) 2 and (second near (floating adj gate)
L4: (380) 3 and (second adj floating)
L5: (197) 4 and (dielectric)
L6: (94) 5 and ((side adj wall) or sidewall)
L7: (83) 6 and (opening\$1 or via\$1 or trench\$
L8: (31) 7 and (opening\$1 or via\$1 or trench\$
L9: (16) 1 and (second adj2 floating adj2 port

Failed

US PAT US 4626

1 and (second adj2 floating adj2 portion\$1)

PT	P	Document ID	Issue Dat	Pages	Title	Current OR	Current (R Retrieval)	Inventor	B	C	F	F	F	F
1		US 20040036108	20040226	18	High coupling floating gate transistor	257/314		Rudeck, Paul						
2		US 20040036106	20040226	18	HIGH COUPLING FLOATING GATE TRANSISTOR	257/314		Rudeck, Paul						
3		US 20030731	20030731	18	Semiconductor device, nonvolatile semiconductor	257/315	257/E21.68	Hayashi, Fumihiko						
4		US 20010015920	20010823	20	Flash eeprom memory cell having increased capacity	365/200	257/E21.20	Ratnam, Perumal et al.						
5		US 20010003366	20010614	19	Semiconductor device, nonvolatile semiconductor	257/315	257/E21.68	Hayashi, Fumihiko						
6		US 6525962	20030225	9	High current and/or high speed electrically contacted cell array	365/185.09	257/314; 257/315	Pai, Sheng-Yueh et al.						
7		US 6243293	20010605	21	Configuration for erasing device and method for multi-level charge/stor	365/185.14	365/185.15	Van Houdt, Jan F. et al.						
8		US 6115285	20000905	21	Contactless array configuration for semiconductor	365/185.03	365/185.2; 365/185.26	Montanari, Donato et al.						
9		US 6009013	19991228	26	Contactless array configuration for semiconductor	365/185.14	365/185.15	Van Houdt, Jan F. et al.						
10		US 5981338	19991109	10	High density flash memory	438/257	438/593	Lee, Roger R.						
11		US 5936275	19990810	9	High density flash memory cell and method	257/315	257/316; 257/366	Lee, Roger R.						
12		US 5841161	19981124	11	Flash memory and method for fabricating the same	257/315	257/321; 257/E21.20	Lim, Min Gye et al.						
13		US 5583810	19961210	13	Method for programming a semiconductor memory	365/185.15	257/319; 257/320	Van Houdt, Jan et al.						
14		US 5410799	19950502	18	Method of making electrostatic switches	29/622	200/181; 29/829	Thomas, Michael E.						
15		US 5389567	19950214	9	Method of forming a non-volatile DRAM cell	438/594	438/251; 438/264	Acovic, Alexandre et al.						
16		US 4672580	19870609	13	Memory cell providing simultaneous non-destructive	365/185.08	257/321; 365/185.1	Yau, Robert L. et al.						